SEMESTER III

II AC I - DIGITAL ELECTRONICS

Internal Marks : 25

External Marks : 75 **Subject Code : UIA1**

Total Marks : 100 **Exam Hrs : 3**

Objectives: To understand the principles of digital logic circuits and their design.

UNIT I

Number Systems – Decimal, Binary, Octal and Hexadecimal systems – Conversion from One System to Another. – Binary Addition, Subtraction, Multiplication and Division – Binary Codes – 8421, 2421, Excess-3, Gray, BCD – Alphanumeric Codes.

UNIT II

Basic Logic Gates – Universal Logic – Boolean Laws and Theorems – Boolean Expressions – Sum of Products – Product of Sums – Simplification of Boolean Expressions – Karnaugh Map Method – Implementation of Boolean Expressions using gate networks.

UNIT III

Combinational Circuits – Multiplexers – Demultiplexers – Decoders – Encoders – Arithmetic Building Blocks – Half and Full Adders – Half and Full Subtractors – Parallel Binary Adder – 2's Complement Adder-Subtractor – BCD Adder.

UNIT IV

Sequential Circuits – Flip Flops – RS NAND Latch - Clocked RS Flip Flop, D Flip Flop, JK Flip Flop, T Flip Flop – Shift Register: Shift Right Register – Shift Left Register – Asynchronous Counter.

UNIT V

D/A and A/D Conversion – Variable Resistor Network – Binary Ladder – D/A Converter – D/A Accuracy and Resolution – A/D Converters – Simultaneous Method – Counter Method – Successive Approximation Method.

Text Book

Albert Paul Malvino and Donald P. Leach, Digital Principles and Applications, Tata McGraw Hill, Fourth Edition, 1996.

SEMESTER III

II AC II - DIGITAL ELECTRONICS LAB

Internal Marks : 40

External Marks : 60 **Subject Code : UIA2Y**

Total Marks : 100 **Exam Hrs : 3**

a) Experiments with Digital IC's

1.Study of Universal IC gates (NAND and NOR) –construction of AND, OR, NOT and EXOR using universal gates.

2. Half adder and full adder (using AND, OR, NOT and EXOR gates only)

3. Half Subtractor and Full Subtractor (Using AND, OR, NOT and EXOR gates only)

4. Karnaugh Map reduction of Boolean Expressions (Three variables expressions only)

5. Study of Shift registers (Serial shift and parallel load)
6. BCD Adder
7. JK Flip Flop

SEMESTER IV

II AC III - E-COMMERCE

SECOND ALLIED COURSE III

Internal Marks : 25

External Marks : 75 **Subject Code : UIA3**

Total Marks : 100 **Exam Hrs : 3**

UNIT I

E-commerce-Electronic Commerce – E-Commerce types – E-Commerce and world at the large-E-Commerce Case studies : Intel , Amazon.

UNIT II

Electronic Mail – The X.400 Message handling system –Internet Addresses – Multipurpose Internet Mail Extension – X.500 Directory Services – E-mail user agent.

UNIT III

EDI- Costs and benefits – Components of EDI Systems – EDI implementation issues – EDIFACT – EDIFACT Message Structure.

UNIT IV

Cyber Security – Cyber Attacks – Hacking- SSL - Authentication and assurance of data integrity – Cryptographic based solutions – Digital Signatures – VPN.

UNIT V

Electronic Payment Systems – payment gateway – internet banking – the SET Protocol – E-cash – E-Cheque –Elements of electronic payments

TEXTBOOK

E-Commerce The Cutting Edge Of Business,Kamalesh K Bajaj, Debjani Nag,McGraw Hill,2011.

REFERENCE BOOK

E-Commerce: Issues, Perspectives and Challenges in the Indian Context, Gupta and Gupta, Knowledge World Publishers,2010.